Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.128”**

**PAD FUNCTION:**

1. **VDD (2 PADS)**
2. **N. STANDBY**
3. **V IN2**
4. **N IN1**
5. **REF OUT/REF IN**
6. **AGND (2 PADS)**
7. **MODE**
8. **DB11 / LOW**
9. **DB10 / LOW**
10. **DB9**
11. **DB8**
12. **DB7**
13. **DB6**
14. **DGND**
15. **DB5 / SDATA**
16. **DB4 / SCLK**
17. **DB3 / N. RFS**
18. **DB2**
19. **DB1**
20. **DB0 (LSB)**
21. **N. RD**
22. **N. CS**
23. **N. EOC**
24. **N. CONVST**

**3 2 1 1 24 23 22**

**21**

**20**

**19**

**18**

**17**

**16**

**10 11 12 13 14 15**

**4**

**5**

**6**

**6**

**7**

**8**

**9**

**.175”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: FLOATING**

**Mask Ref: D92C**

**APPROVED BY: DK DIE SIZE .128” X .175” DATE: 5/17/21**

**MFG: ANALOG DEVICES THICKNESS .019” P/N: AD7892A-1**

**DG 10.1.2**

#### Rev B, 7/19/02